Understanding the basics of setup and hold time

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To understand why setup and hold time arises in a flip-flop one needs to begin by looking at its basic function. These flip-flop building blocks include inverters and transmission gates. Inverters are used to invert the input. It is important here to note its characteristic voltage transfer curve (See Figure 1).

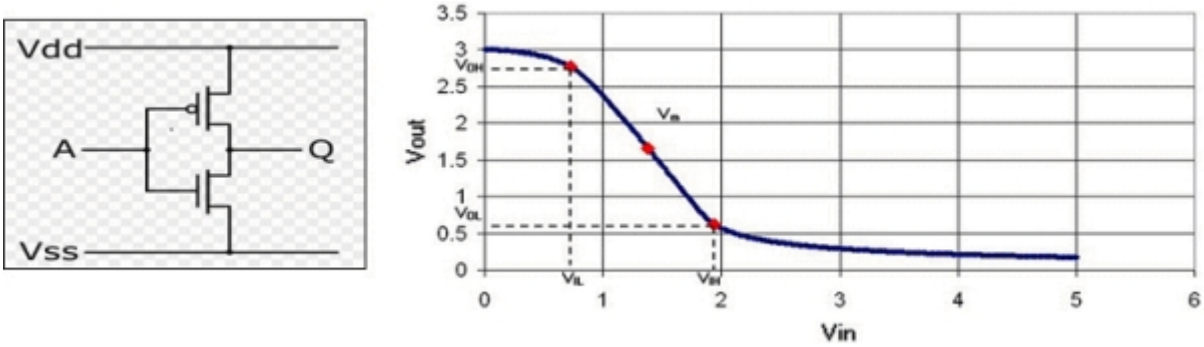
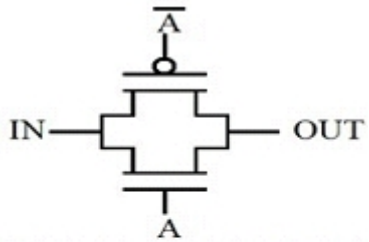


Figure 1. A basic building block of a flip-flop, an inverter features a characteristic voltage transfer curve.

A transmission gate, denoted by Tx throughout the article, is a parallel connection of nMOS and pMOS with complementary inputs to both MOSFETs (see Figure 2). Bidirectional, it carries current in either direction. Depending on the voltage on the gate, the connection between the input and output is either low-resistance or high-resistance, so that Ron = 100 Ω or less and Roff > 5 MΩ. This effectively isolates the output from the input.



CONTROL		INPUT	OUTPUT
pMOS	nMOS	IN	OUT
0	1	0	0
		1	1
1	0	0	Z
		1	

Figure 2. A transmission gate, shown here with a truth table, is a parallel connection of

nMOS and pMOS with complementary inputs to both MOSFETs.

Whenever both nMOS and pMOS are turned on, any signal '1' or '0' passes equally well without degradation. The use of transmission gates eliminates undesirable threshold voltage effects which give rise to loss of logic levels.

The transistor level structure of a D flip-flop contains two 'back-to-back' inverters known as a 'latching circuit,' since it retains a logic value. Immediately after the D input, an inverter may or may not be present (See Figure 3).

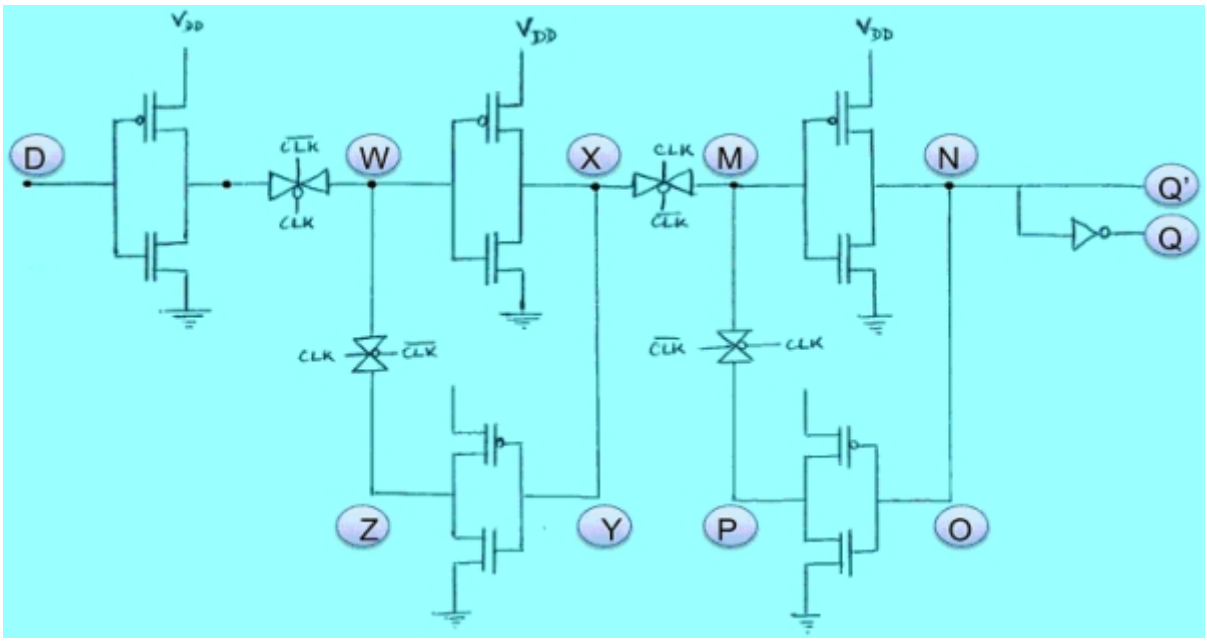


Figure 3. The transistor level structure of D flip-flop contains two back-to-back inverters known as a'latching circuit.

Normal operation of a flip-flop

In order to visualize normal operations of a flip-flop (See Figure 4), in 4a, initially D = 0 and CLK is LOW. Input follows the path D-W-X-Y-Z and finally Z = 0. We are neglecting the 'latching circuit' on RHS for the time being.

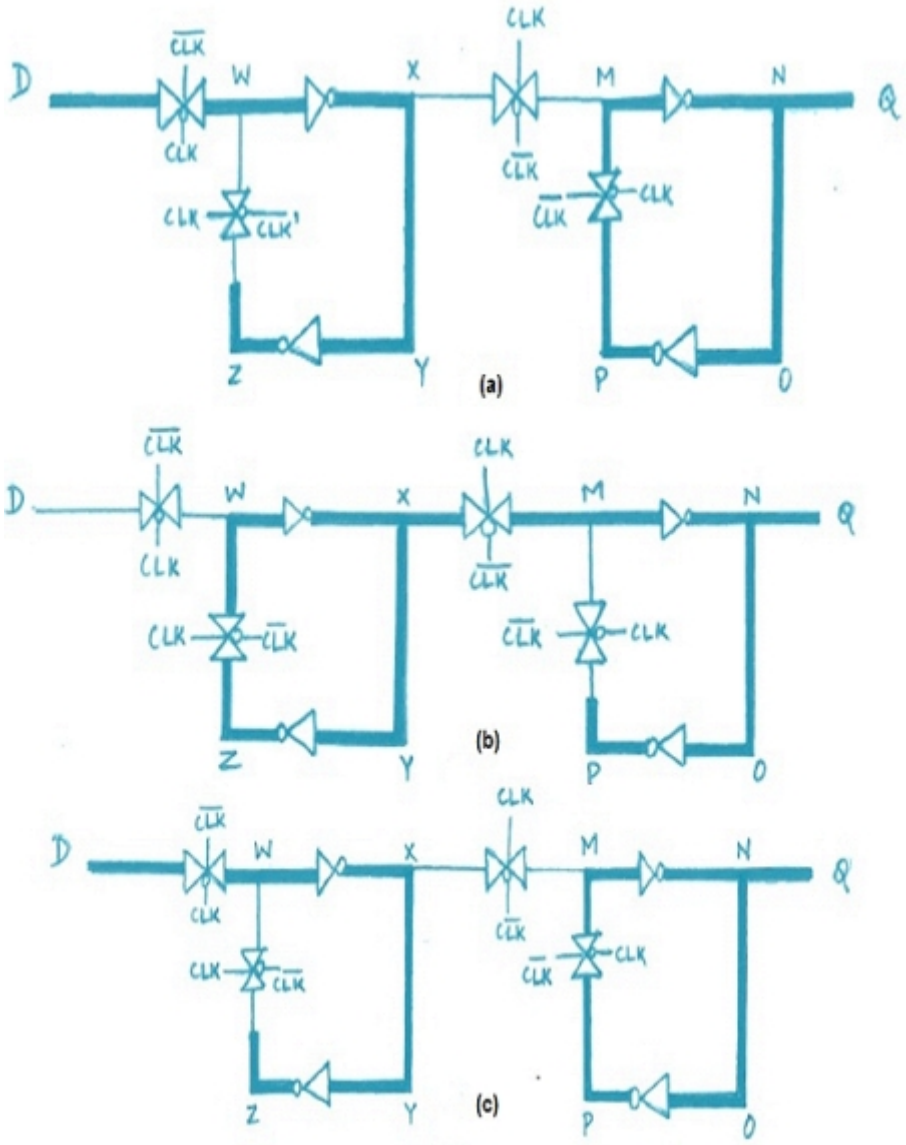


Figure 4. The workings of a D flip-flop whereby the darkened line shows the conducting path.

When the CLK is HIGH (See 4b), latching circuit on LHS is enabled. It latches 1, which results in Q = 0 (which is what it should be for D = 0). Note that the output arrives at the positive edge of CLK. Hence it is a positive edge triggered flip-flop.

When the CLK is LOW, the RHS latching circuit is enabled (See 4c) and there is no change in output. Any change in input is reflected at node Z which is reflected in the output at the next positive edge of CLK.

In summary, if D changes, the change would reflect only at node Z when CLK is LOW and it would appear at the output only when the CLK is HIGH.

It is here that we introduce SETUP and HOLD time. Setup time is defined as the minimum amount of time before the clock's active edge that the data must be stable for it to be latched correctly. Any violation may cause incorrect data to be captured, which is known as setup violation.

Hold time is defined as the minimum amount of time after the clock's active edge during which data must be stable. Violation in this case may cause incorrect data to be latched, which is known as a hold violation. Note that setup and hold time is measured with respect to the active clock edge only.

Reason for SETUP Time:

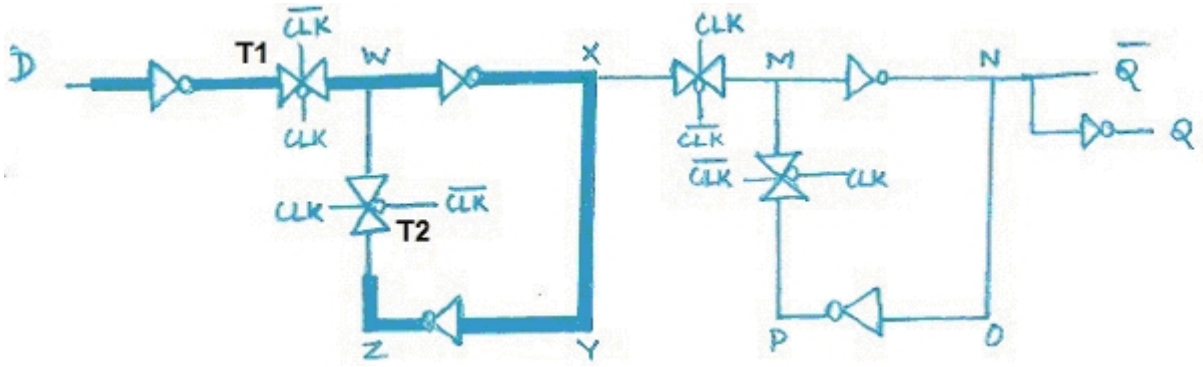


Figure: 5. The time it takes data D to reach node Z is called the setup time.

In Figure 5, when D = 0 and CLK is LOW, input D is reflected at node Z so that W = 1, Y = 0, and Z = 1 and it will take some time to traverse the path D-W-X-Y-Z. The time that it takes data D to reach node Z is called the SETUP time. When the CLK is HIGH, T1 is switched OFF and T2 is switched ON. Therefore, the LHS 'latching circuit' kicks into action latching the value present at node Z, and producing it in the output (Q = 0 and Q' = 1).

It is indispensable for node Z to have a stable value by then. Any data sent before the setup time, as defined above, will produce a stable value at node Z. This defines the reason for the setup time within a flop.

Reason for HOLD Time:

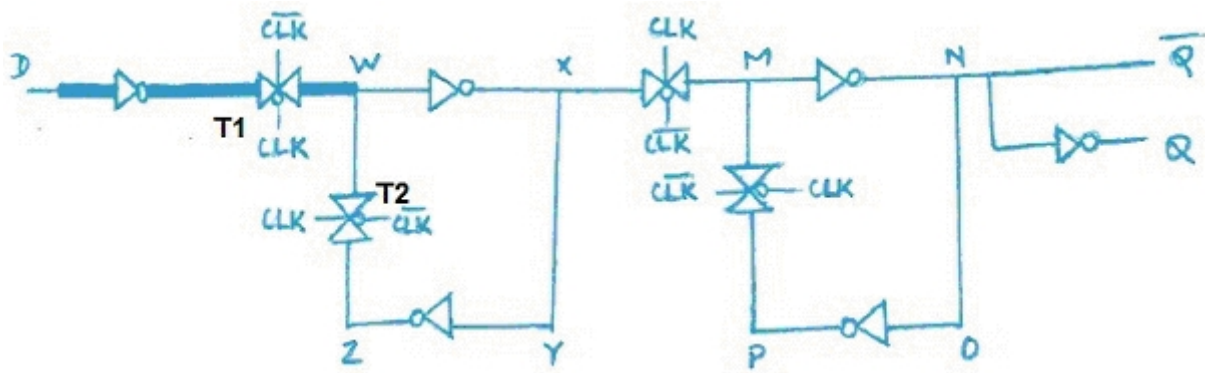


Figure 6. The darkened line shows the conducting path for hold time.

As previously indicated, HOLD time is measured with respect to the active CLK edge only. In Figure 6, input data D is given to the inverter, or any other logic sitting before transmission gate T1, and is a part of the flip-flop. The CLK and CLK BAR in Figure 6 that controls the switching of the transmission gates, come after the ramping up of the CLK signal, i.e. after passing through buffers and inverters.

There is a finite delay between the CLK and CLK BAR so that the transmission gate takes some time to switch on or off. In the meantime it is necessary to maintain a stable value at the input to ensure a stable value at node W, which in turn translates to the output, defining the reason for hold time within a flop.

A finite positive setup time always occurs, however hold time can be positive, zero, or even negative. Let's look at why and how this can be true. As discussed earlier, there may be combinational logic

sitting before the first transmission gate to make the flop set-reset-enable or scan-enable, possibly for yet another reason. This introduces a certain delay in the path of input data D to reach the transmission gate. This delay establishes whether the hold time is positive, negative, or zero.

In Figure 7, Tinitial is the time delay introduced by the combinational logic sitting before the first transmission gate and TTX is the time taken for the transmission gate to switch ON or OFF after the CLK and CLK BAR is given. The relationship between Tinitial and TTX gives rise to the various types of hold time that exist.

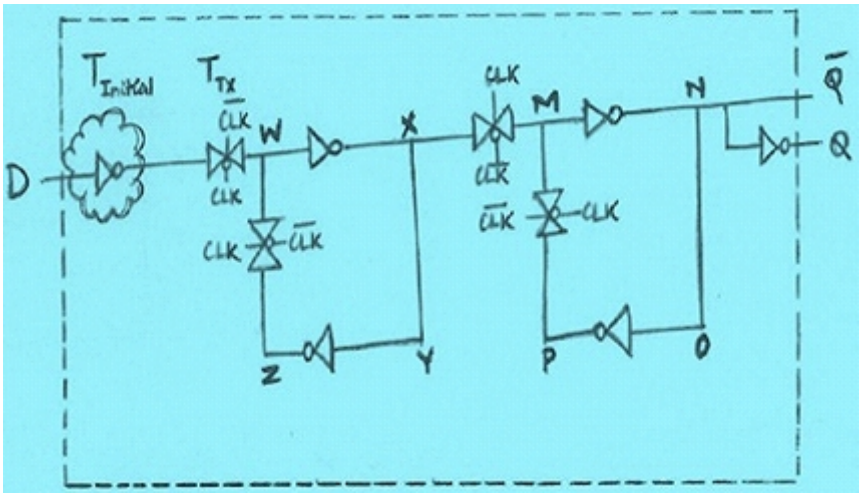


Figure 7. The relationship between Tinitial and TTX establishes various types of hold time

The relationship between Tinitial and TTX in Figure 8 further clarifies positive, zero, and negative hold time.

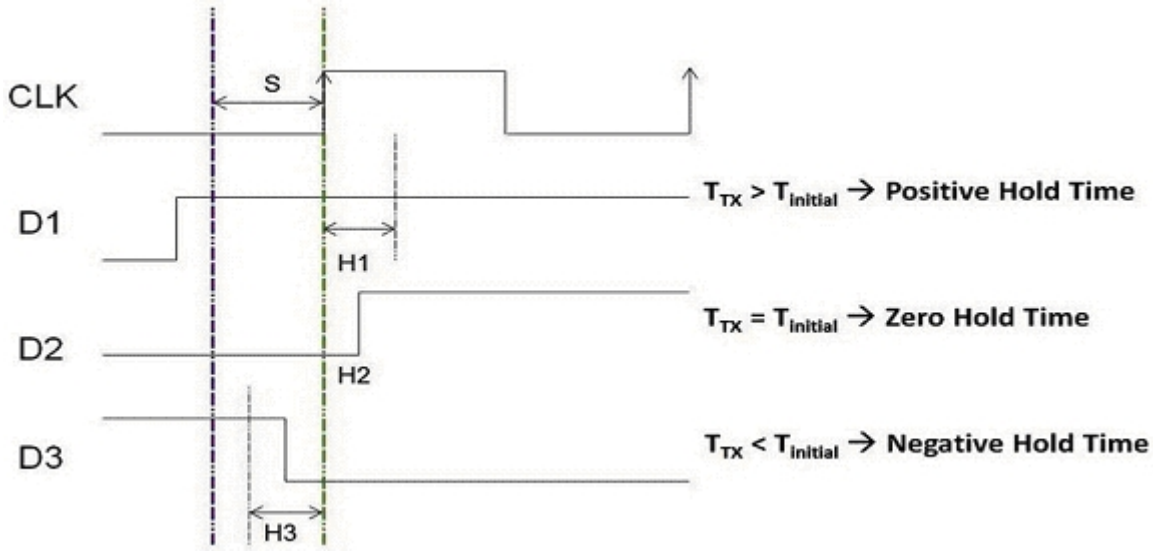


Figure: 8. Relationships that establish positive, zero, and negative hold time. Adjusting the TTX changes the hold margin.

In Figure 8, CLK represents the clock with an active rising edge, D1, D2 and D3 represent various data signals, S represents the setup margin, and H1, H2, and H3 denotes the respective hold margins. TTX indicates the time taken for the transmission gate to switch ON or OFF after the CLK and CLK BAR arrive, and Tinitial is the time delay introduced by the combinational logic sitting before the first transmission gate. Since HOLD margin is always decided with respect to the active clock edge, playing with the TTX will change the hold margin.

About the authors:

Deepak Behera is a design engineer with experience in signal integrity and package designing and analysis. Karthik Rao C.G. is a design engineer with experience in digital IP design. Deepak Mahajan is a design Engineer with experience in SoC verification.